REMARKS

The application includes claims 1-24 prior to entering this amendment.

The examiner rejects claims 1-24 under 35 U.S.C. § 102(e) as being anticipated by Litt (U.S. Patent 7,051,239).

The applicant amends claim 13 to correct a typographical error.

The application remains with claims 1-24 after entering this amendment.

The applicant adds no new matter and requests reconsideration.

Claim Rejections Under § 102

The examiner rejects claims 1-24 as being obvious over Litt. The applicant traverses the rejection for the following reasons.

Litt discloses a system in which an on-chip logic analyzer (OCLA) 125 is included in an integrated circuit 100.[1] During debug modes, one or more sets of an on-chip cache memory 150 are disabled from use by other circuitry in the integrated circuit, and reserved exclusively for use by the OCLA 125. Data stored in the reserved cache set can then be read out by the OCLA 125, and placed in a register that can be accessed by other logic internal or external to the integrated circuit.[1]

Claim 1 recites *creating error conditions responsive to the intercepting* and *transmitting the error conditions*. Claim 13 includes a similar limitation. The examiner alleges that "Litt discloses a system that can test a process over bus lines with an OCLA used to test data on a cache over a bus."[2] The examiner, however, fails to specifically point out where Litt discloses creating error conditions responsive to the intercepting. Litt's OCLA is "capable of reading the data from the cache memory to a register that can be addressed by the processor,"[3] thereby "providing a robust history log for debugging and performance testing of the integrated circuit."[4] Litt, however, does not disclose creating error conditions in the data read from the cache memory, as would be required by claims 1 and 13. For at least this reason, claims 1 and 13 should be in condition for allowance, along with associated dependent claims.

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[1] Litt, abstract, figure 1.
[2] Office action dated 4/9/2007, page 2, paragraph 3b.
[3] Litt, column 7, lines 53-57.
[4] Litt, column 4, lines 54-59.

Claim 2 recites *dropping selected data packets*. Claims 8, 14, and 20 include similar limitations. The examiner alleges that "Litt discloses a system with ability to test bus routing of data from the OCLA to the cache."[5] The examiner, however, does not specifically point out where Litt discloses dropping selected data packets. As discussed before, Litt's OCLA 125 may read out data from cache set 150 and place it in a register that can be accessed by other logic. Litt, however, does not disclose dropping selected data packets to create an error condition, as would be required by claims 2, 8, 14, and 20. For at least this reason, claims 2, 8, 14, and 20 should be in condition for allowance.

Claim 3 recites *creating error conditions* including *intentionally corrupting selected data packets*. Claims 9, 15, and 21 include similar limitations. The examiner alleges that Litt discloses a system wherein an OCLA tests memory address problems by having faulty address call. According to Litt:

"...the OCLA memory addresses are given an I/O space non-cacheable address, but those addresses are routed to the cache memory. Routing the OCLA address range to the cache memory, however, will not be sufficient to drive out the data because the address will not match any address tags in the cache controller, unless the address tags associated with cache set x are loaded in the cache controller and maintained as valid at all times so that the cache controller cannot invalidate or evict the data."[6]

That is, Litt discloses that the OCLA address range may not match address tags in the cache controller because the OCLA memory addresses are given an I/O space non-cacheable address. Litt, however, does not disclose *corrupting selected data packets* to *create error conditions*, as would be required by claims 3, 9, 15, and 21. And hence, Litt cannot disclose *intentionally* corrupting selected data packets, as recited in these claims. For at least these reasons, claims 3, 9, 15, and 21 should be in condition for allowance.

Claim 5 recites *analyzing traces stored in a trace buffer*. Claim 17 includes similar limitations. The examiner alleges that "Litt discloses a system wherein data is sent from an OCLA and receiving data, filtering it, and using it to determine operational status of the system."[7] The examiner's allegations are not clear to the applicant. Litt recites the word "buffer" only once in his disclosure, where he refers to a "history buffer".[8] Litt does not disclose a trace buffer. And hence, Litt can not disclose analyzing traces stored in a trace buffer, as would be required by claims 5 and 17.

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[5] Office action dated 4/9/2007, page 2, paragraph 4.
[6] Litt, column 12, lines 13-22, underline added.
[7] Office action dated 4/9/2007, page 3, paragraph 7.

Claim 7 recites *means for identifying data packet* and *means for modifying the data packets responsive to the identifying*. Claim 19 includes similar limitation. As discussed with respect to claim 1, Litt's OCLA is "capable of reading the data from the cache memory to a register that can be addressed by the processor,"[3] thereby "providing a robust history log for debugging and performance testing of the integrated circuit."[4] Litt, however, does not disclose *identifying data packets* and *modifying the data packets responsive to the identifying*, as would be required by claim 7. For at least this reason, claims 7 and 19 should be in condition for allowance, along with associated dependent claims.

Claim 10 recites *identifying two or more sequential data packets having a predetermined type*. Claim 22 includes similar limitations. The examiner alleges that Litt discloses a system wherein data is sent to an OCLA and receiving data and filtering it so it can be used in the debug mode. Although Litt's OCLA 125 "acquires internal processor state as data, and stores selected state data in the pre-selected cache memory set(s),"[9] Litt does not disclose identifying *two or more sequential data packets having a predetermined type*, as would be required by claims 10 and 22.

Conclusion

For the foregoing reasons, the applicant requests reconsideration and allowance of the remaining claims. The applicant encourages the examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,
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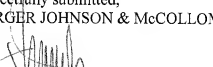

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[8] Litt, column 3, lines 9-10.
[9] Litt, column 8, lines 34-36.